Ballistic Transport Modeling in Nano-MOSFETs

H. Achour A. Benfdila
LMPDS, Faculty of Electrical and Computer Engineering,
The University M. Mammeri, Tizi-Ouzou, Algeria

In electronic devices, electronic transport is achieved by diffusion and through the drift of carriers to as far as the electric field to which they are subjected to and which is far from causing hot carriers and the total path greater than 50 nm. When the device dimensions are drastically reduced, the carrier transport in the conducting layers cannot be free from the field effect. Hence, carrier over-acceleration occurs and hot carriers are created. Hot carriers (electrons or holes) will produce damages in the conducting channel material inducing the loss of the excess energy. This occurs especially in short channel MOSFETs.

In the recent development of integrated circuits, devices are reduced to the nano-scale dimensions and the carrier transport is no more classical. Quantum and ballistic effects are observed and then related models are used for modeling carrier transport in these devices.

The major transport phenomenon is the ballistic transport, which occurs in deep submicron MOSFETs of channel length less than 50nm. However, for channel length higher but closer, there is no method that can evidence the occurrence or non-occurrence of the ballistic phenomenon.

In the present work, we deal with the modeling of ballistic current transport in nano-MOSFEs. The current modeling is based on the Natori and Landauer approaches.

Simulations of the drain-source current are achieved for various conditions of bias and dimension after a ballistic MOSFET modeling.