

A Study of Erasing in Programmable Electrically Erasable Read Only Memory (EEPROM) with Very Thin Oxide Tunnel

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1. Introduction

The use of EEPROM (Programmable Electrically Erasable Read Only Memory) covers these last years a large range of applications in electronics such as EPLD (Electrically Programmable Logic Devices) and ASIC (Application Specific Integrated Circuits). For this reason, the EEPROM cell performance is has been a subject of many studies.

In this paper, we present a model developed under VHDL AMS language (Very High Speed Integrated Circuits Hardware Description Language), it describes the operation of erasing in this type of memory. The model is a synthesis between the models level 1 and 3 of SPICE language. The aim of this study is the optimization of this cell in order to support a maximum number of cycles of erasing and writing operations.

2. Main results

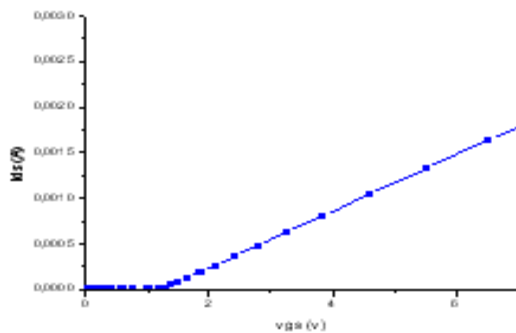


Fig.1: Characteristic $i_{ds} = F(V_{gcs})$ in linear mode of a virgin cell.

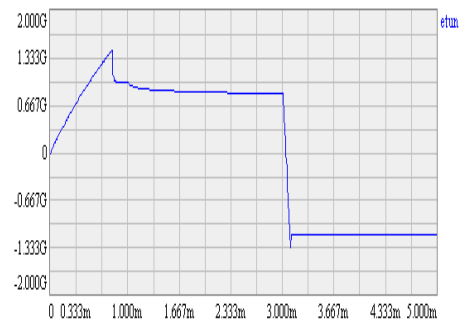


Fig.2: The electrical field between the floating gate and the drain $E_{tun} = F(t)$.

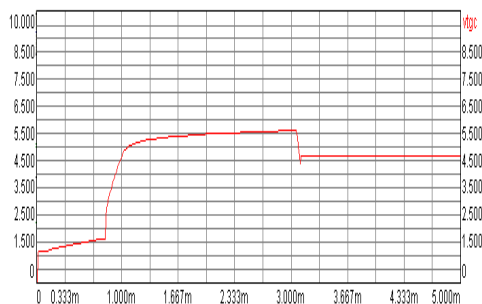


Fig.3: The variation of the threshold voltage during the operation of erasing $V_{tgc} = F(t)$.

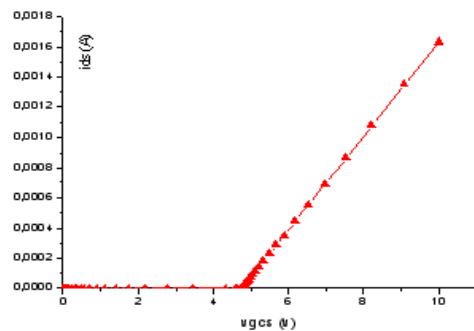


Fig.4: Characteristic $i_{ds} = F(V_{gcs})$ after erase operation.

3. Conclusion

We have developed compact model of an EEPROM cell. In this model, we have seen a strong coupling that exists between the control gate and the floating one during the operation of erasing.

We could see also an increase in the voltage V_{tgc} threshold during erasing. This variation is due to the presence or absence of a charge in the floating gate. The sign, as well as the quantity of this charge, is a determining factor on the value of V_{tgc} . The injection of this charge through the oxide tunnel induces a progressive degradation of the quality of this one.

This model can be used for study of the electrical properties of the cell. It allows the simulation of both transient and static characteristics. This model, implemented in circuit simulators, offers the capability to simulate the complete transient programming and to follow the shift of the threshold voltage and the amount of the charge trapped on the floating gate as a function of time programming.