

On the Signal Propagation Delay Study for the Deep Submicron CMOS Integrated Circuit

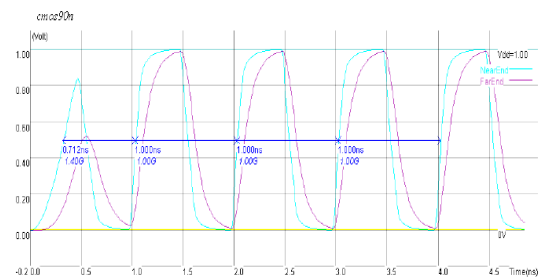
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1. Introduction

The continuous scaling of transistors combined with an increased chip area results in the ratio of global wire delay to gate delay increasing at a super-linear rate. For sub-0.25 μm technology and multi-gigahertz clock frequencies [1], on-chip interconnects may exhibit transmission line behaviour [2]. In this paper, we present with some detail a study of the signals propagation delay due to the crosstalk noise in modern deep submicron integrated circuits (ICs). Interconnects have become a potential bottleneck for further improvements in circuit speed because their performance are limited by parasitic effect like the RC behaviour of the wires. These last are defined by their geometries, material types and by their encountered dielectrics.

2. Main results

Let us consider a wire with length L, delimited by two gates “Near End” and “Far End”. We analyze the signal propagation for two different technologies. The first one is *CMOS012* and the second one is *CMOS90n* [3]. We simulate the signal propagation in this wire by using *MICROWIND* software [4]. The simulation results are given by the following figures.

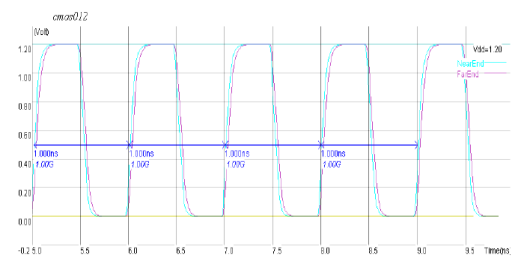


(b)

Fig.1: Simulation result of signal propagation delay for cmos012 (a) and cmos90n (b).

From these simulation results, it is clear that the dimensions reduction cause a signal propagation delay that can be a serious difficulty for signal synchronization. Moreover, such problem can yields a total modification in circuit behaviour.

A solution for improvement in the signal propagation is to insert repeaters. This method yields the following results: In order to exhibit this effect, we have analysed the signal propagation delay for an integrated circuit in *CMOS035* technology. This simulation is performed for two different transistors, the first one is the Level3 (SPICE model) and the second one is the BSIM4. Simulation results are given by the following figures.



(a)

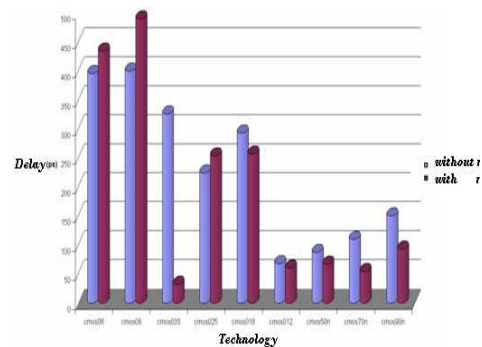


Fig.2: Simulation result of signal propagation with and without repeaters.

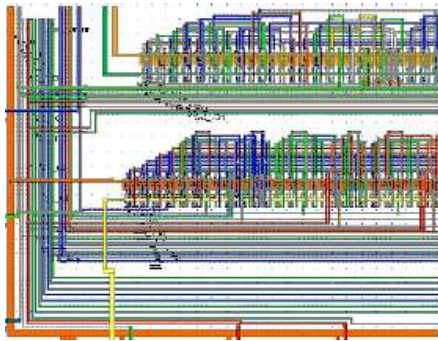


Fig.3: Part of the simulated circuit.

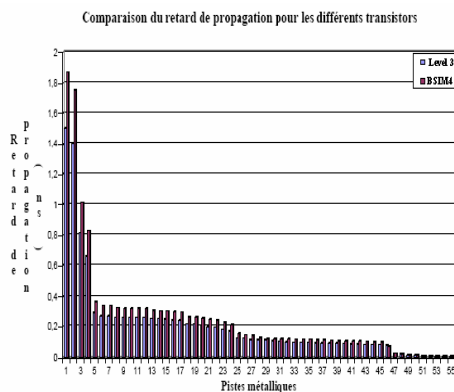


Fig.4: Simulation result of signal propagation delay for different transistors.

3. Conclusion

Signal integrity is one of the most critical problems that the VLSI design community faces today. Crosstalk delay is the major factor in signal integrity issues for the latest process technology nodes. With the present technological evolution, the study of signal propagation become a very important step in systems conception.

Regarding design new routing strategies that better account for transmission line effects, the introduction of ground planes or shielding wires will help to control on-chip inductive effects and signal propagation. The introduction of Copper and new dielectrics can enhance and speed up the signal propagation.

References

- [1] Paolo Ciampolini et al., "Advanced models for the Simulation of Interconnections in VLSI Circuits", p.106 (2002).
- [2] Rainer Sabelka, Christian Harlander and Siegfried Selberherr, "Interconnects and

Propagation of high Frequency Signals", p.357 (2003).

- [3] Rul Martins et al., IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, **17**, No.11, 1148 (1998).
- [4] Satyendra Ravi Prasad Raju Datla, "Crosstalk delay analysis in very deep sub-micron VLSI circuits", Master Thesis, Southern Methodist University, May (2004).