Role of $^{+19}$F Implantation to Grow Multiple Gate Oxides For Nano-CMOS Technology

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A novel technique of growing oxides of multiple thicknesses Grow-Etch–Implant and Re-grow (G-E-I-R) using fluorine implantation in Silicon for the nano-metric gate oxide technologies was used. Fluorine as compared to nitrogen and oxygen enhances the oxidation rate of silicon and improves the interface and bulk properties of the MOS devices. In this paper, growth of ultra thin multiple oxides with different thicknesses using G-E-I-R approach on the same wafer to vary the threshold voltage (V_t) and reduction of effective oxide charges(Q_{EFF}) with low energy fluorine ion implantation and its electrical characterization results are presented.

1. Introduction

Driven by Moore's law, microelectronics has gone through many integration levels in the last many decades [1]. At present, the level of integration is such that it is not the integration of single function circuits on a chip, but instead it is the integration of multi function circuits into so called a system on chip (SOC). In SOC, it is required to integrate various modules such as digital, analog, I/O, RAM, and power management circuits and others [2].

Integrating these diverse modules on the same chip is understandably a challenging task for technology. One such challenge is the ability to grow the gate dielectric films of varying thicknesses, such as silicon dioxide on a single chip.

Imai et al. have reported triple gate technologies where a thin gate oxide is grown for the core logic and pass transistors, a thicker oxide for the lower power CMOS areas and an even a thicker gate oxide for the I/O modules [3]. The analog circuit requirements are very often in conflict with the digital circuit requirements [2]. All this demand the ability to grow gate oxides of multiple thicknesses in the nano-metric regime. Different techniques to grow multiple gate oxide thicknesses have been proposed in the literature over the last few years [4-5]. Togo et al. proposed the implantation of Argon and Nitrogen for dual gate CMOS field-effect transistor in SOC fabrication [6]. Unlike the nitrogen, the argon implantation was found to enhance the oxidation rate [7]. The argon implantation at a dose of 1×10^{15} ions/cm^2 was found to increase the leakage current and a decrease in time to break down (T_{BD}). It has been demonstrated in the case of nitrogen implantation that there is a trade-off between the amount of nitrogen incorporation, which in turn decides the gate oxide thickness, and the gate oxide reliability [7]. The higher implants doses of nitrogen give better thickness control but cause degradation of gate oxide reliability [8].

Hinriches et al. attempted oxygen implantation and demonstrated that severe damages occur in the substrate casting oxygen implantation as an unsuitable technique for forming gate oxides [9]. Enhancement in the oxidation rate due to different halogens (fluorine, iodine) and xenon species was compared for different oxidation and implant conditions [10]. Fluorine-implanted silicon after annealing is expected to leave less residual damages due to its smaller size as compared to the other halogens. Not many attempts have been reported in the literature on fluorine implantation with the view of changing the oxide thickness for SOC applications in the nano-metric scale. In the present work, the low energy fluorine ions have been implanted at varying doses to control the oxidation rate, and thereby the thickness of the grown ultra thin oxides. This technique could be used to grow multiple thickness gate oxides for SOC applications.

2. Experimental

RCA cleaned p-type silicon wafers of 10-30 Ω-cm resistivity and <100> orientation were used for these experiments. The Grow-Etch-Implant-Regrow (G-E-I-R) technique was used to grow nano-metric regime oxide thicknesses. The oxide thickness of 8.1nm was initially grown on three

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sample sets in the furnace at 900ºC using dry oxygen. After oxidation, wafers were spun coated with positive photoresist and masked to expose the 3/4th of the wafer towards the major flat. After developing, the wafers were dipped in 1:50 (40%HF+H_2O) for 20 seconds to etch oxide from ¾th part of wafer. The pre-grown oxide portion and the portion where no implantation was to be made were masked with photoresist. The unmasked portions were implanted with $^{19}F^+$ at a dose of 1×10^{14}, 2×10^{14} and 2.5×10^{14}ions/cm^2 (Implant-1). Then wafers were again implanted with $^{19}F^+$ at a dose of 2×10^{14} and 2.5×10^{14} ions/cm^2 (Implant-2).

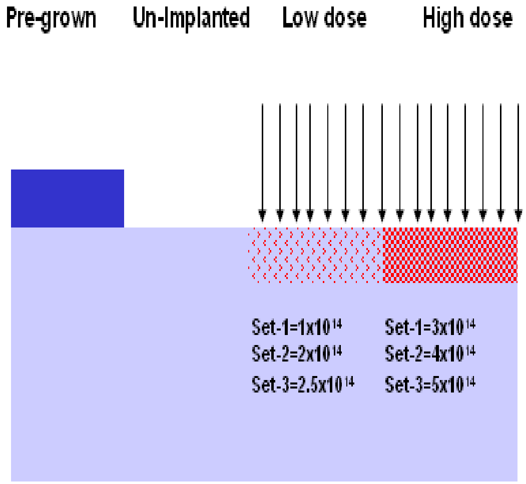

Fig.1

Then the wafers were split into four sets: pre grown, un-implanted, implanted with $^{19}F^+$ Low Dose, and implanted with $^{19}F^+$ High Dose as shown in Fig.1. Oxidation was carried out in the furnace at 800^{0}C for 5 minutes and obtained thicknesses of 2.0 nm, 2.1 nm, 2.2 nm, 2.3 nm, 2.5 nm, 2.7 nm, 3.0 nm and 8.1nm as measured using Rudolf Research's Ellipsometer (Auto EL-III).The MOS capacitors of 100µm×100µm area were fabricated and electrically characterized at room temperature by capacitance-voltage (C-V) at 1 MHz frequency and current-voltage (I-V) measurements using a Keithley 590 C-V Analyzer, 230 Voltage Source and 2602 Keithley Source meter.

3. Results and discussions

Fig.2 indicates the C-V characteristics of MOS devices measured for Pre-grown and for oxide films grown on p-type silicon before and after fluorine implantation at a low and high doses, respectively. The gate voltage was swept from inversion to accumulation [+5V to -5V] during these measurements. The different values of capacitances for these samples may be attributed to difference in oxide thickness or to a possible change in the dielectric constant of grown oxide due to the incorporation of fluorine. However, the second possibility was ruled out by measuring the oxide thickness using Ellipsometry. The oxide thickness was measured from Ellipsometry and obtained using the CV measurements. The result clearly indicates that the measured thicknesses are same within the experimental error.

So, the change in capacitance is due to the change in oxide thickness rather than due the change in the dielectric constant. This clearly indicates that the oxidation rate has increased after fluorine implantation. Capacitance-Voltage (C-V) curve of MOS based on Pre-grown oxide indicates a flat band voltage (V_{FB}) shift towards the negative voltage axis indicating the presence of high density of fixed positive charges (+Q) in the pre-grown silicon oxide film. The un-implanted region shows a flat band voltage shift towards positive voltage axis. The pre-grown SiO_2 layer was etched using HF based etchant. This treatment forms Si-F (silicon-fluorine) network as previously observed by Kasi et al. [11] and results in a significant shift of the flat band (V_{FB}) voltage due to the reduction of fixed oxide charges with in the thin dielectric films. The low energy (10 keV) fluorine ion implantation, both at low and high doses, shifts the flat band voltage along the positive direction of voltage axis.

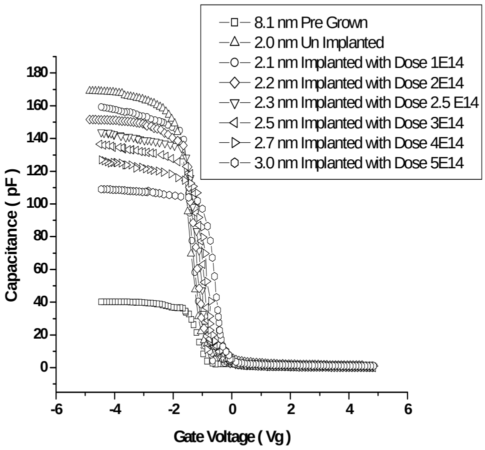

Fig.2

The flat band voltage shift from pre-grown oxides to the fluorine implanted gate oxides indicates the flexibility of altering the flat band voltage (V_{FB}) with low energy fluorine ion implantation. As indicated in Fig.3, a significant change in the threshold voltage (V_t) and the effective oxide charge (Q_{EFF}) of pre-grown, un-implanted and fluorine implanted samples is observed [13].

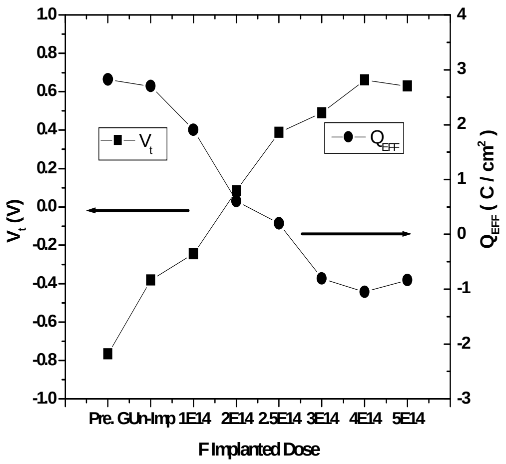

Fig.3

There could be fixed positive charges within the pre-grown oxide. The incorporation of fluorine is expected to compensate the fixed positive charges thus resulting in the change of threshold voltage. Even in the case of un-implanted samples, there could be significant fluorine incorporation due to HF treatment [12]. The threshold voltage (V_t) is calculated by the following relation:

$$V_t = \left[\pm \frac{A}{10^{12} C_{ox}} \sqrt{4\varepsilon_s q \left|N_{BULK}\right| \left|\phi_B\right|} + 2\left|\phi_B\right| \right] + V_{FB}$$

Here C_{ox}, Φ_B, V_{FB}, ε_s, q, N_{BULK} and A are threshold voltage, oxide capacitance, bulk potential, flat band voltage, permittivity of silicon, electronic charge, bulk-doping concentration, and electrode area respectively .

There is a decrease in the effective oxide charge due to fluorine incorporation in the oxide. The shift in the flat band voltage in the positive direction with fluorine ion implantation and reduction in the oxide charges implies that fluorine implantation contributes negative charges. Maegawa et al. reported a similar behavior of the fluorine ion implantation in gate oxides [12]. Fig.4. shows the gate leakage current density of MOS capacitors as a function of gate voltage (V_g). As evident from the figure, there is a significant reduction in the gate leakage current with the gate voltage for increased dose of fluorine ions. It is attributed to a reduction in the gate oxides defects [14]. Fig.5 shows the distribution of interface state density (D_{it}) in the Si band gap before and after fluorine incorporation within the oxide.

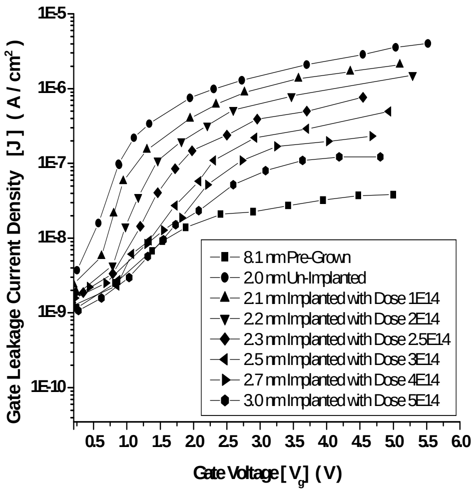

Fig.4

The interface trap density versus energy curve examines the trap densities near the mid gap (E_t).

The interface trap energy from mid gap, E_t, is measured as the difference of silicon surface potential (ψ_s) and bulk potential (¢_B). The interface traps density (D_{it}) is calculated from the interface state capacitance (C_{it}) using the following relation:

$$D_{it} = \frac{(1\times10^{-12})C_{it}}{Aq}$$

The interface trap density of fluorine ion implanted samples was less than that of un-implanted oxides samples. This measurement also implies an improvement in the quality of oxide due to the reduction of interface state density.

Fig.6 shows a schematic diagram of fluorine effects on the SiO_2 structure. The Si/SiO_2 interface is re-oxidized by the released oxygen atoms consequent on the breaking of Si-O bonds due to fluorine incorporation. This result indicates an increase in oxide thickness that occurs mainly at the Si/SiO_2 interface.

4. Conclusion

This paper describes (G-E-I-R) technique to grow ultra thin multiple gate oxides in the nano-metric regime using low energy fluorine ion implantation for SOC technologies. It is found that the oxidation rate increases with fluorine ion dose and the threshold voltage has been found to vary with the dose. This could have possible applications in controlling the threshold voltage in addition to conventionally used channel doping. There is a marked improvement in the quality of gate oxide as shown by the results on effective oxide charges, gate leakage current and the interface trap density. So, fluorine implantation could be a useful alternative technique of growing varying oxide thicknesses, especially the ultra-thin oxides for SOC technology.

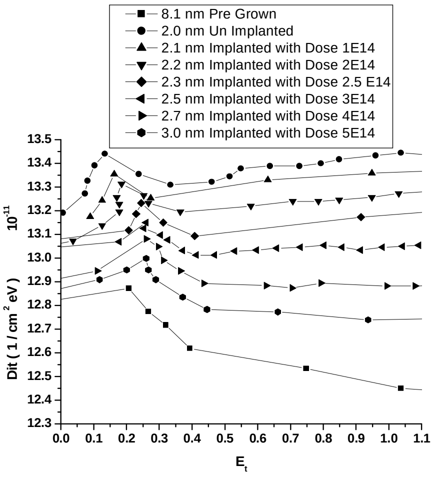

Fig.5

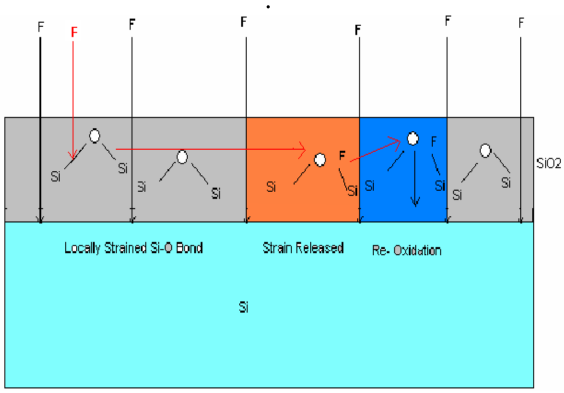

Fig.6

Acknowledgments

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